REMARKS

The specification has been amended to correct typographical errors and does not present new matter. Claims 13-19 have been amended, claims 1-8 and 12 have been canceled, and claims 20-28 have been added. Thus, claims 9-11 and 13-28 remain pending in the case. Further examination and reconsideration of the presently claimed application is hereby respectfully requested.

Duplicate Claim Warning

Claims 1 and 15 were objected to under 37 CFR 1.75 as being substantial duplicates of one another. The Examiner's thorough review of the claims is appreciated. To expedite prosecution, claim 1 and all dependent claims therefrom have been canceled rendering objection thereto moot. Accordingly, removal of this objection is respectfully requested.

Section 101 Rejection

Claims 1, 8, 9, and 15 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. As noted above, claims 1 and 8 have been canceled rendering rejection thereto moot. As set forth below, Applicants respectfully traverse the Examiner's rejection of present claims 9 and 15, and request that this rejection be reversed.

With regard to the rejection of claim 1, the Examiners suggests that the preamble term "system" is ambiguous, and that the claimed "state restoration logic" appears to be a data structure per se, which would fall into the category of non-statutory subject matter (Office Action, page 5). The Examiner further suggests that claims 9 and 15 should be rejected for the same reasons as claim 1 (Office Action, page 5). However, neither claim 9 nor claim 15 include the term "system" within the preamble or claim limitations, and, therefore, cannot be rejected for including the so-called ambiguous term. Claim 9 also fails to include the "state restoration logic" limitation, which the Examiner assumes to be a (non-statutory) data structure, and, therefore, cannot be rejected for doing so. Applicants are merely confused as to why claim 9 is "rejected for the same reasons as claim 1" when claim 9 fails to include any of the terms or limitations rejected by the Examiner for claim 1.

Though claim 15 recites a limitation on "state restoration logic," it is improper for the Examiner to assume that any and all recitations of "logic" should be limited to software-implemented logic only. Rather, and as is known in the art, "logic" may be implemented in hardware, as well as software. In one example, hardware implementations of logic may include a single logic element (e.g., a logic gate, register, selection element, etc.) or combinations of logic elements. In one embodiment of the invention, the "state restoration logic" recited in claim 15 may be implemented with a multiplexer (i.e., a selection element) coupled between the state machine and the backup register. As such, the multiplexer may be coupled for receiving a current state of the state machine (from the state machine) and a previous state of the state machine (from the backup register). Depending on the state of a control signal, the multiplexer may select the current state or the previous state of the state machine as output. For example, if a trigger event generated by the microprocessor is invalid, the control signal may cause the previous state to be selected so that the state machine can be properly restored to its preceding state. Support for the hardware-implementation of the presently claimed "state restoration logic" may be found, e.g., in the Specification, on page 17, lines 4-19; in Fig. 5 of the drawings; and in newly added claims 23-28.

For at least the reasons set forth above, Applicants believe that the §101 rejection of claims 9 and 15 is improper. Accordingly, removal of this rejection is respectfully requested.

Section 112, 2nd Paragraph, Rejections

Claims 1, 3, 12, and 15 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As noted above, claims 1, 3, and 12 have been canceled rendering rejection thereto moot. To expedite prosecution, the preamble of claim 15 has been amended to recite a "microprocessor comprising a diagnostic module," instead of a "microprocessor with an associated diagnostic module." This amendment is believed to clarify the claim language in a manner that addresses the concerns expressed in the Office Action. Accordingly, removal of this rejection is respectfully requested.

Section 103 Rejections

Claims 1-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Engineering Approach to Digital Design* by William I. Fletcher, Prentice Hall, Inc., 1980, pages 276-279 (hereinafter "Fletcher") in view of Advanced Microprocessors by Daniel Taback, McGraw-Hill, Second Edition, 1995, pages 28, 67, 139, 145, 363 and 466 (hereinafter "Taback"). As noted above, claims 1-8 and 12 have been canceled rendering rejection thereto moot. As set forth below, Applicants respectfully traverse the § 103(a) rejections levied against claims 9-11 and 13-19.

To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03 (emphasis added). Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d. 1382 (CCPA 1970). Using these standards, Applicants contend (i) that the hypothetically combined cited art fails to teach or suggest all features of the currently pending claims; and (ii) that the references cannot be hypothetically combined since there is no impetus or motivation described in those references to form the combination suggested in the Office Action. Several distinctive features of the present invention are set forth in more detail below.

Fletcher and Taback fail, both individually and in combination, to teach, suggest or provide motivation for a diagnostic module including: (i) a state machine, which is adapted to change its internal state in response to trigger events generated by the microprocessor, and to halt the microprocessor in response to a trigger event and a preceding internal state prior to the trigger event, and (ii) state restoration logic adapted to use a backup register to restore the state machine to its preceding state, if a trigger event is invalid. Independent claim 15 recites, in part:

> A microprocessor comprising a diagnostic module, said module comprising: a state machine adapted to change its internal state in response to trigger events generated by the microprocessor, and adapted to halt the microprocessor in response to a trigger event and a preceding internal state prior to the trigger event; a backup register... and state restoration

logic adapted to use the backup register to restore the state machine to its preceding state, if the trigger event is invalid.

Independent claim 9 recites a similar limitation. As such, claims 9 and 15 provide a microprocessor and method for saving and restoring states of a state machine (or diagnostic module), depending on whether a trigger event generated by the microprocessor is valid or invalid. Examples of valid and invalid trigger events can be found throughout the specification and present claims 25 and 27.

Statements in the Office Action suggest that the term "state machine" is disclosed by Fletcher, the terms "restore" and "state restoration logic" are disclosed by Taback and, thus, "it would have been obvious to a person of ordinary skill in the art to use Taback to modify Fletcher." (Office Action, page 7). The Applicants disagree with the Examiner's attempt to oversimplify the claim limitations by ignoring the functional limitations of the presently claimed "state machine" and "state restoration logic." As set forth in more detail below, Fletcher and Taback each fail to teach, suggest or provide motivation for the presently claimed "state machine" and "state restoration logic," as actually recited in claim 15 and, thus, cannot be combined or modified to do so.

On page 7 of the Office Action, the Examiner suggests that the term "state machine" is disclosed by Fletcher on page 279 ("FINITE STATE MACHINE") and on page 276, which states, "[a] model of a controlled system with feedback is shown in Figure 5-2. By using this feedback, *ideally the output of a controlled system at some time t_o is the resultant of both the input conditions at t_o, combined with all the input conditions leading up to t_o.*" (Taback, pages 276 and 279, emphasis original).

With regard to page 279 of Fletcher, Applicants assert that the mere mention of a "state machine" is insufficient evidence to render the presently claimed "state machine" unpatentable. Applicants wish to remind the Examiner that "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d. 1382 (CCPA 1970). By simply pointing to the words "FINITE-STATE MACHINE" on page 279 of Fletcher, the Examiner clearly fails to consider all words recited in the claim and, therefore, fails to provide sufficient evidence of teaching within Fletcher for the presently claimed "state machine," which is specifically adapted "to change its internal state in response to trigger events generated by the microprocessor, and to halt the microprocessor in response to a trigger event and a preceding internal state prior to the trigger event."

The Examiner also points to page 276 of Fletcher, which describes a control system with feedback, to provide teaching or suggestion for the presently claimed "state machine." The Applicant disagrees and asserts that there is absolutely no teaching, suggestion or motivation for the presently claimed "state machine" on page 276 of Fletcher. Fletcher simply fails to disclose the "state machine" as set forth in present claim 15 and, therefore, cannot be relied upon to do so.

On page 7 of the Office Action, the Examiner suggests that the terms "restore" and "state restoration logic" are disclosed on page 363 of Taback, which states, "[a]fter a return, and when the register file was out of windows, we have a window underflow. Software must restore previously used register windows in this case. A window overflow trap is caused by the overflow." As such, the Examiner appears to suggest that the "software" disclosed on page 363 of Taback is somehow equivalent to the presently claimed "state restoration logic." The Applicant disagrees.

The "software" disclosed by Taback functions to restore previously used register windows, whose contents are saved in memory in response to a window overflow, and restored after a return when a window underflow condition exists (*see*, Taback, page 363). Even if one were to falsely assume that the stored "contents" of Taback's "register windows" were somehow equivalent to the stored "preceding state" of the presently claimed "state machine," Taback does not disclose that the "contents" may be restored in response to an invalid trigger event. As far as Applicants can tell from the information provided, Taback teaches that the "contents" are restored when an "underflow" condition occurs, i.e., when the number of currently running active windows is less than the maximum number of windows (e.g., NWINDOW = 8) available for use. If this is true, the "underflow" condition described by Taback cannot be considered equivalent to an "invalid trigger event," which is described in the specification and present claims as a condition that occurs, e.g., when a branch instruction is re-executed after returning from an exception associated with an instruction immediately following the branch instruction. Since Taback fails to provide teaching or suggestion for an "invalid trigger event," as described in the present claims, Taback cannot provide teaching or suggestion for "state restoration logic adapted to use the backup register to restore the state machine to its preceding state, if the trigger event is invalid."

For at least the reasons set forth above, Fletcher fails to provide teaching or suggestion for the presently claimed "state machine," or any other limitation set forth in the present claims. In addition, the present limitations, including the presently claimed "state restoration logic," are not taught or suggested by Taback. The Examiner suggests that the teachings of Taback can be used to modify the teachings of

Fletcher. The Applicants disagree, and assert that there is absolutely no suggestion or motivation within the cited art that would enable one skilled in the art to modify or combine the teachings of Fletcher and Taback to produce the claimed invention. Furthermore, even if the cited art references were combined (without sufficient motivation to do), the combined teachings of the cited art would still fail to disclose all limitations of present claims 9 and 15.

For at least the reasons set forth above, none of the cited art, either individually or in combination, teaches, suggests or provides motivation for all limitations of independent claims 9 and 15. Therefore, Applicant's assert that independent claims 9 and 15, and all claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

Patentability of Added Claims

The present amendment adds dependent claims 20-28. Support for the added limitations may be found in the specification, e.g., on page 4, lines 6-19; page 10, line 10 to page 12, line 13; page 13, lines 6-17; page 17, lines 4-26; in original claims 4-8, 16 and 17; and in Fig. 5 of the drawings. Since claims 20-28 are dependent on claim 15, claims 20-28 are patentably distinct for at least the same reasons set forth above for the patentability of claim 15. Accordingly, approval of added claims 20-28 is respectfully requested.

CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed February 10, 2005. In addition, the prior art cited but not relied upon is not considered to be pertinent to the presently claimed case. In view of the remarks traversing the rejections, Applicants assert that pending claims 9-11 and 13-28 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to LSI Logic Corp. Deposit Account No. 12-2252.

Respectfully submitted,

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